13. Advanced Fan-Out Developments and Applications

Course Leaders: John Hunt and Jan Vardeman – TechSearch International, Inc.

Course Description:
Fan-out wafer-level packaging (FO-WLP) has evolved from a low-cost packaging option for automotive and mobile applications to a high-performance computing packaging solution. Both chip-first and chip-last solutions have been adopted and are expanding in complexity to serve a range of applications including AI training and inferencing, replacing silicon with an organic redistribution layer (RDL) as the interposer. The potential for packaging for RF and photonics is also described. The course provides a brief overview of the various fan-out packages, a history of their evolution, and discussion of the current structures and reasons for adoption in each application. Differences between the three basic processes flows: Chip First Die Down, Chip First Die Up, and Chip Last are explained with examples of each structure. Bridge solutions are described, including process flows, advantages, and applications. The course also discusses the move to large panels for cost-reduction and discusses both the potential advantages and challenges. Production examples and process flows are included.

Course Outline:

1. Overview: Drivers for Fan Out
2. Basic Low-density Fan Out
3. 3D Fan Out Structures
4. High Density Die to Die Fan Out
5. Fan Out Embedded Bridge Technology
6. Fan Out System in Package
7. Antenna in Package
8. Fan Out Silicon Photonics Integration
9. Fan Out Memory Packaging
10. Panel Fan Out

Who Should Attend: Anyone interested in understanding Fan-out wafer-level packaging and the differences between the various FO-WLP structures. Individuals interested in understanding the advantages of the various types of fan-out for different applications. Engineers and managers who would benefit from an understanding of the landscape of package options, advantages, and alternatives.

Bio 1: John Hunt is a Senior Analyst with TechSearch International, Inc. He has more than 50 years of experience in a wide variety of positions with semiconductor processing, semiconductor packaging, and the manufacturing and testing of electronic components and systems, with emphasis on the development of new technologies and processes. His previous position was with ASE, where he spent more than 21 years working with the factories to develop and bring to manufacturing all aspects of wafer level packaging, including the introduction of Wafer Level Chip Scale Packaging, and the full spectrum of Fan Out Packaging. He has a B.S. degree from Rutgers University and a joint M.S./MBA degree from the University of Central Florida. He received the IMAPS Daniel C. Hughes, Jr. Memorial Award in 2023 and is an IMAPS Fellow.

Bio 2: E. Jan Vardaman is president and founder of TechSearch International, Inc., which has provided market research and technology trend analysis in semiconductor packaging since 1987. She is the co-author of How to Make IC Packages (by Nikkan Kogyo Shinbunsha), a

columnist with Printed Circuit Design & Fab/Circuits Assembly, and the author of numerous publications on emerging trends in semiconductor packaging and assembly. She served on the NSF-sponsored World Technology Evaluation Center (WTEC) study team involved in investigating electronics manufacturing in Asia and on the U.S. mission to study manufacturing in China. She is a senior member of IEEE EPS and is an IEEE EPS Distinguished Lecturer and received the Distinguished Achievement Certificate for Technical Leadership and Expertise in May 2024. She received the IMAPS GBC Partnership award in 2012, the Daniel C. Hughes, Jr. Memorial Award in 2018, the Sidney J. Stein International Award in 2019, and she is an IMAPS Fellow. She has served on the IEEE CPMT Board of Governors for two terms. Before founding TechSearch International, she served on the corporate staff of Microelectronics and Computer Technology Corporation (MCC), the electronics industry's first pre-competitive research consortium.